**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-22 (cancelled)

Claim 23. (previously presented) A twin MONOS NAND memory array, comprising:

a) an array of twin MONOS memory cells arranged in rows and columns and forming a NAND memory array,

b) a word gate located over two storage sites of each memory cell of said memory cells,

c) a diffusion forming a source and a drain connecting between said memory cells in a column

d) a first selector gate located at top of a column and connected to a first memory cell in said column.

e) a second selector gate located at a bottom of a column and connected to a last memory cell in said column

Claim 24. (previously presented) The memory array of claim 23, wherein said word gate is a part of a word line, which is further a row of said word gates.

Claim 25. (previously presented) The memory array of claim 23, wherein said source and said drain are formed by a single diffusion located between adjacent memory cells in said column.

Claim 26. (previously presented) The memory array of claim 23, wherein said storage sites are nitride elements located below said word gate.

Claim 27. (previously presented) The memory array of claim 23, wherein said first and second selector gates select said column of memory cells to allow memory operations to be performed.

Claim 28. (previously presented) The memory array of claim 23, wherein said diffusions in rows are isolated from each other by a shallow trench isolation.

Claim 29. (currently amended) A NAND memory array using twin MONOS memory cells, comprising:

a) a means ~~to~~ for ~~locate~~locating two storage sites under each word gate of a twin MONOS memory array,

b) a means for connecting together said word gates in a row of said memory array,

c) a means for connecting together a plurality of memory cells in a column of said memory array, wherein said column has an upper voltage and lower voltage,

d) a means for selecting said upper voltage to be connected to said column,

e) a means for selecting said lower voltage to be connected to said column,

f) a means for performing memory operations by selecting said upper and lower voltages and by applying a plurality of voltages to the word gates of said plurality of cells in said column.

Claim 30. (previously presented) The memory array of claim 29, wherein said storage sites are nitride structures extending beneath said word gates.

Claim 31. (previously presented) The memory array of claim 29, wherein said means for connecting word gates together in a row is a word line deposited across said memory array and forming the word gates of each memory cell in said row.

Claim 32. (previously presented) The memory array of claim 29, wherein said means for connecting together said plurality of memory cells in a column is through a diffusion formed between each memory cell of said plurality of cells in said column.

Claims 33-61 (cancelled)